REMARKS

Prior to entry of the present amendment, claims 1-65 were pending in the present application. Claims 1-53 and 57-64 are canceled above. Claims 54 and 65 are amended above. New claims 66-114 are added above. No new matter is added by the claim amendments. Entry is respectfully requested.

With reference to new claims 66-114 added above, it is submitted that the new claims are all readable on the previously identified sub-species of group A, "memory systems with claimed operations based on clock signals".

Claims 1-4, 6-9, 11 and 60-61 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth (U.S. Patent No. 6,029,250). Claim 5 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth, and further in view of Gasbarro, *et al.* (U.S. Patent No. 5,432,823). Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Moyal, *et al.* (U.S. Patent No. 6,326,853). Claim 12 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Wada, *et al.* (U.S. Patent No. 6,029,250). Claims 13-15 and 22-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Yoshitake (U.S. Patent No. 6,043,704). Claim 57 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Gillingham, *et al.* in view of Keeth and further in view of Chan, *et al.* (U.S. Patent No. 5,998,860). Reconsideration and removal of the above rejections are respectfully requested, in view of the cancellation of claims 1-53 and 57-64.

Claims 54-56 and 65 stand rejected under 35 U.S.C. 102(e) as being anticipated by Gillingham, *et al.* (U.S. Patent No. 6,510,503). Reconsideration and removal of the rejections and allowance of claims 54-56 and 65 are respectfully requested.

With regard to the rejection of independent claims 54 and 65, in the present invention as claimed in independent claim 54, a memory system having a stub configuration includes a controller for generating a first clock signal, a memory module including memory devices coupled to the controller, and a second clock signal generator independent of both the controller and the memory module for generating a second clock signal. The memory module receives the first clock signal and the second clock signal.

In the present invention as claimed in independent claim 65, a method of transferring data in a memory system having a stub configuration includes generating a first clock signal at a controller, and generating a second clock at a second clock signal generator independent of both the controller and a memory module including memory devices coupled to the controller. The method further includes receiving the first clock signal and the second clock signal at the memory module.

Gillingham, *et al.* fails to teach or suggest a memory system that includes "a controller for generating a first clock signal", "a memory module including memory devices coupled to the controller", and a "second clock signal generator independent of both the controller and the memory module for generating a second clock signal", as claimed in claim 54. Instead, in Gillingham, *et al.*, during a read operation, memory devices 84 drive one of the data clocks dclk0 and dclk1 in a source synchronous manner along with read data on the databus and the controller 82 schedules which of the data clocks should be used, such that the controller knows which data clock to use to latch in read data. Therefore, Gillingham, *et al.* does not disclose a "second clock signal generator independent of both" a "controller" and a "memory module" as claimed in claim 54. Further, Gillingham, *et al.* fails to teach or suggest a method of transferring data in a memory system that includes "generating a second clock at a second clock signal generator independent" of "both" a "controller" and a "memory module", as claimed in claim 65. Instead, in Gillingham, *et al.*, during a read operation, memory devices 84 drive one of the data clocks dclk0 and dclk1 in a source synchronous manner along with read data on the databus and the controller 82 schedules which of the data clocks should be used, such that the controller knows which data clock to use

to latch in read data. Reconsideration and removal of the rejection of claims 54 and 65 under 35 U.S.C. 102(e) as being anticipated by Gillingham, *et al.* are therefore respectfully requested. With regard to the dependent claims 55 and 56, it follows that these claims should inherit the allowability of the independent claims from which they depend.

With regard to newly added claims 66-114, it is submitted that the cited references, whether alone, or in combination, fail to teach or suggest the invention as claimed. Entry and allowance of the newly added claims are respectfully requested.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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